UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,872	03/01/2002	Yukiko Morishita	245402004500	6071

7590 07/31/2003

Madeline Johjnston
Morrison & Foerster LLP
755 Page Mill Rd.
Palo Alto, CA 94304-1018

EXAMINER
TRAN, CHUC

ART UNIT	PAPER NUMBER
2821	

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/087,872	MORISHITA, YUKIKO
	Examiner	Art Unit
	Chuc D Tran	2821

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,10,11,13,14,16 and 17* is/are rejected.

7)☒ Claim(s) *4,7,9,12,15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5-6, 8, 10-11, 13-14, and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Hatano et al (USP. 5,432,808).

Regarding claim 1, Hatano disclose a compound semiconductor light emitting device comprising:

- a mount member (43) having a mount surface (fig. 8);
- the semiconductor light emitting device chip (44) is connected to the mount surface of the mount member (43) by solder between the semiconductor light emitting device chip (44) and the mount surface of the mount member (Fig. 8) (Col. 10, Line 30); and
- the mount member (43) includes a material (GaAlInN) (Col. 6, Line 20) higher in thermal expansion coefficient than a material for the chip substrate (42) (Fig. 8) (Col. 4, Line 40) (Col. 10, Line 27-32).

Regarding claim 3, Hatano disclose that the chip substrate (42) includes nitride based compound semiconductor (Col. 5, Line 6) (Col. 10, Line 28).

Regarding claim 5, Hatano disclose that the solder includes In (Col. 5, Line 9).

Regarding claims 6 and 8, Hatano disclose that the chip substrate (42) includes nitride based compound semiconductor (Col. 5, Line 6) (Col. 10, Line 28).

Regarding claims 10 and 13, Hatano disclose a semiconductor light emitting device comprising:

- a mount member (43) having a mount surface (Fig. 8);
- the semiconductor light emitting device chip (44) is connected to the mount surface of the mount member (43) by solder between the semiconductor light emitting device chip (44) and the mount surface of the mount member (Fig. 8) (Col. 10, Line 30); and
- the mount member (43) includes a material (GaAlInN) (Col. 6, Line 20) higher in thermal expansion coefficient than a material for the chip substrate (42) (Fig. 8) (Col. 4, Line 40) (Col. 10, Line 27-32);
- the stack is formed by semiconductor light emitting device (44) to the mount surface of the mount member (43) (Fig. 8).

Regarding claims 11 and 14, Hatano disclose that the chip substrate (42) includes nitride based compound semiconductor (Col. 5, Line 6) (Col. 10, Line 28).

Regarding claim 16, Hatano disclose a semiconductor light emitting device comprising:

- a mount member (43) having a mount surface (fig. 8);
- the semiconductor light emitting device chip (44) is connected to the mount surface of the mount member (43) by solder between the semiconductor light emitting device chip (44) and the mount surface of the mount member (Fig. 8) (Col. 10, Line 30); and
- the mount member (43) includes a material (GaAlInN) (Col. 6, Line 20) higher in thermal expansion coefficient than a material for the chip substrate (42) (Fig. 8) (Col. 4, Line 40) (Col. 10, Line 27-32);
- the stack is formed by semiconductor light emitting device (44) to the mount surface

of the mount member (43) (Fig. 8); wherein

- the mount surface (43) are connected by solder of In (Col. 5, Line 9).

Regarding claim 17, Hatano disclose that the chip substrate (42) includes nitride based compound semiconductor (Col. 5, Line 6) (Col. 10, Line 28).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano.

Regarding claim 2 differ from Hatano in that they all call for various conventional die bonding, cladding methods by using a compressive force is applied to a stack for curving the semiconductor laser chip. However, the inclusion of these methods does not render the claims patentably distinct over Hatano in view of the fact that these methods are well accepted practice for in cladding, die bonding structures. Thus, it would have been obvious to anyone of ordinary skill in the art to choose any of the above conventional methods for forming Hatano's structure in view of its convenient.

Allowable Subject Matter

3. The indicated allowability of claim 5 is withdrawn in view of the newly discovered reference(s) to Hatano. Rejections based on the newly cited reference(s) follow.

Claims 4, 7, 9, 12, 15 & 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

1. The following is a statement of reasons for the indication of allowable subject matter:

Prior art fails to disclose the mount member includes at least one of iron and copper posses all of the distinctive features such as defined by claims 4, 7, 9, 12, 15, and 18 to improve thermal conductivity.

Response to Arguments

4. Applicant's arguments filed 5/16/03 have been fully considered but they are not persuasive.

Applicant argues that the patent by Hatano does not disclose the chip substrate as recited in the claims and the mount member is connected to the semiconductor light emitting device chip by solder. The Examiner respectfully disagree. The Hatano. clearly disclose the chip substrate (42) (Fig. 8) (Col. 4, Line 40) as recited in the claims and the mount member (43) is connected to the semiconductor light emitting device chip (44) (Fig. 8) by solder, cladding, die bonding (Col. 10, Line 30) (die bonding as recited in the Applicant's specification page 19, Line 12).

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuc D Tran whose telephone number is (703)306-5984. The examiner can normally be reached on M-F Flex hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on (703)308-4856. The fax phone numbers for the

organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

TDC
July 28, 2003

Don Wong
Supervisory Patent Examiner
Technology Center 2800